<u>IN THE CLAIMS</u>:

The listing of the claims will replace all prior versions, and

listings, of claims in the application:

Listing of Claims:

Claim 1 (Currently Amended): A system for transmitting data

in a serial bidirectional bus with a control device comprising

a send and receiving unit for data fields combined into a

data frame, and

with bus subscribers connected in series which comprise an

evaluation circuit for reading in and reading out data fields in

data frames,

<u>wherein each bus subscriber (2, 3, 4) comprises a test</u>

<u>circuit (24) to determine whether it is located at the bus end</u>

<u>opposite of the control device,</u>

with at least the bus subscriber at the bus end ~~opposite of~~

~~the control device~~ comprising a send device for a data frame,

wherein at least the bus subscriber (4) at the ~~end of the~~

bus <u>end</u> comprises a control stage (13) which is activated by a

received data frame (6) sent by the control device (1) <u>over the</u>

<u>serial bidirectional bus</u> and triggers the send device (12)

depending on the receipt of a data frame (6)

for sending a data frame (11) <u>over the serial bidirectional</u>

<u>bus</u> in the direction of the control device (1) whereas the sent

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data frame (11) contains at least data fields (14, 15, 16) for all bus subscribers (2, 3, 4) and said data frame (11) is handed over from one bus subscriber to the next bus subscriber.

Claim 2 (Previously Presented): A system according to claim 1,

wherein each of the bus subscribers comprises a control stage (13) for a send device (12) for sending a data frame (11) for the own data fields and the data fields of the bus subscribers which lie between the control device (1) and the respective bus subscribers.

Claim 3 (Previously Presented): A system according to claim 1,

wherein the bus subscribers (2, 3 and 4) comprise a memory (14) for the position of the data fields (7, 8, 9, 14, 15 and 16) within the respective data frame (6, 11), which data fields can be read in and out via the evaluation circuit (10).

Claim 4 (Previously Presented): A system according to claim 3,

wherein the control device (1) comprises an allocation stage (17) for the position of the data fields (7, 8, 9,14, 15 and 16)

within a data frame (6 or 11) which can be allocated to the
individual bus subscribers (2, 3 and 4) and an initialization
device (18) for reading out the positional data in data fields of
a data frame addressed to the individual bus subscribers, and
that the bus subscribers (2, 3 and 4) comprise an initialization
circuit (23) for the address-related reading out of the
positional data from the addressed data fields of the data frame
into the memory (14) for these positional data.

Claim 5 (Previously Presented): A system according to claim
1,

wherein each bus subscriber (2, 3 and 4) comprises a test
circuit (24) for recognizing a bus subscriber (3 and 4) connected
to the bus (5) and connected in outgoing circuit with the same.

Claim 6 (Previously Presented): A system according to claim
1,

wherein, as is known, the control device (1) and the bus
subscribers (2, 3 and 4) each comprise an encoding device (25)
for producing check data (16) from the data frame (6 and 11), and
that, as is known, the control device (1) and the bus subscribers
(2, 3 and 4) each comprise a check device (27) for check data
received with the data frames (6 and 11).

Claim 7 (Previously Presented): A system according to claim 1,

wherein the control device (1) comprises an address memory (30) for the addresses (31) of the bus subscribers and that each bus subscriber (2, 3 and 4) comprises a recognition circuit (32) for triggering the evaluation circuit (10) for reading out the data field (20, 21 or 22) in the data frame (19) addressed to the bus subscriber (2, 3 or 4) on the one hand and for reading in its data field (28, 29 or 30) into the data frame (27) on the other hand.

Claim 8 (New): A system according to claim 1,

wherein multiple data fields are sent simultaneously in a single data frame and at a time.